Partial and Dynamic Reconfiguration of FPGAs: a top down design methodology for an automatic implementation

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Abstract

Dynamic and partial reconfiguration of FPGAs enables systems to adapt to changing demands. This paper concentrates on how to take into account specificities of partially reconfigurable components during the high level Adequation Algorithm Architecture process. We present a method which generates automatically the design for both partially and fixed parts of FPGAs.

1. Introduction

The recent and next generations wireless systems (802.11 up to 4G) are being designed to provide a wide variety of multimedia services and seamlessly switch between different wireless standards. Most Software Defined Radio solutions are based on Digital Signal Processors (DSPs) combined with Field Programmable Gate Array (FPGAs). The split between Hardware/Software components during the partitioning process leads to a compromise between system's performance of an hardwired solution and flexibility of a software solution. Reconfigurable devices, including FPGAs, can fill the gap between hardwired and software technology. Recently runtime reconfiguration of FPGA parts has led to the concept of virtual hardware. This technic allows to change only a specified part of the chip while other areas remain operational and unaffected by the reconfiguration [3]. In this paper we focus on reconfiguration methodology for FPGAs, based on AAA approach and associated tool SynDEx [1]. The way of modeling a partially runtime reconfigurable part of a FPGA with SynDEx is exposed. A case study is presented in last section followed by the conclusion.

2. Reconfiguration Levels

In the case of mobile communications, three main constraints have to be combined : high performance, low power consumption and flexibility. Three levels of reconfiguration can be considered :

- System Level Reconfiguration : In this case, the application is very often supported by an heterogeneous architecture. Either, these hardware solutions do not allow the reconfiguration of the datapath.
- Functional Level Reconfiguration : Some FPGAs support partial dynamic runtime configuration. A function can be replaced by another one while other parts stay operative. A runtime reconfiguration manager will control, monitor and execute the dynamic reconfiguration.
- Logic and RTL level Reconfiguration : The majority of the FPGAs are fine grain. Switching the configuration of a design is very quick, as the bitstream differences are smaller than the entire bitstream. Neither, this level is architecture's manufacturer dependant and do not allow the designer to adopt an open methodology.

Considering the SDR constraints, the functional reconfiguration level seems to be the best level for our partial and dynamically reconfiguration of systems.

3. Design flow for dynamic reconfiguration : AAA approach

Some partitioning methodologies based on various approaches are reported in the literature [2]. Among theses methods we have chosen the AAA approach. AAA methodology aims at finding the best matching between an algorithm and an architecture while satisfying time constraints. SynDEx automatically generates a distributed and

optimized synchronized executive. The reader is referered to previous works [1] which describe all the steps of the methodology and extensions to FPGAs modelization. Figure 1 depicts the overall methodology flow. The mapping and scheduling of the operations and data transfers onto the operators and the communication media are carried out by a heuristic which takes into account durations of computations and inter-component communications.

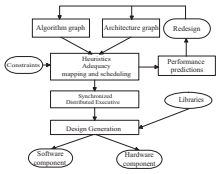

Figure 1. SynDEx methodology flow

To reduce the difficulty in managing such dynamic reconfigurable application and to provide reliable implementation, following issues must be adressed : automatic or manual partitioning of an application, specification of the dynamic constraints, automatic generation of the C or VHDL core controler. Considering these features in SynDEx, runtime reconfigurable parts of a FPGA (D1 and D2) and fixed parts (F1) can be represented as hardware operators of the architecture. (D1 and D2) will integrate both dynamic modules and the control to manage the reconfiguration.

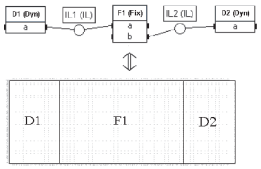

Figure 2. Model of runtime reconfigurable parts of a FPGA with SynDEx

Reconfiguration of the dynamic part is performed by two sub-parts: a Configuration manager and a Protocol configuration builder. The Configuration manager is in charge of the configuration bitstream which must be loaded on the reconfigurable part by sending configuration requests. Reconfigurations are performed as soon as the reconfigurable part is unused. Configuration requests are sent to the Protocol configuration builder which is in charge to construct a valid reconfiguration stream. Encapsulation of operators with a standard interface allows to reconfigure only the area containing the operator without altering the design around. Functionalities involved in the general control of the dynamic area and control manager remain all the time in the static part. These two operators are automatically generated by SynDex and translate in VHDL with our libraries. In our design flow, the Xilinx Modular Design back-end flow is used to place and route each module and to generate the associated bitstream.

4. Case study : MC-CDMA reconfigurable transmitter

Our top-down design flow has been used to design a transmitter system based on MC-CDMA modulation scheme [4]. This transmitter is implemented on a prototyping board with a FPGA Xilinx Xc2v2000 which integrates an internal reconfiguration access port(ICAP) for partial reconfiguration .

The FPGA is divided in two parts. The first one is static and implements non reconfigurable logic, the second one is dedicated to the dynamic operator.The self reconfiguration operates at 20Mhz, one bistream byte is loaded each cycle by the ICAP. The reconfiguration time needed takes about 4ms. As the maximum net bit rate per user is about of 0.296Mbits/s, time to reconfigure the modulation is of the order of some data frames. Additional details and informations will be given during the poster presentation.

5 Conclusion

A methodology flow to manage automatically partially reconfigurable parts of a FPGA has been proposed. The AAA methodology and associated tool SynDEx have been used to perform mapping and automatic code generation for fixed and dynamic parts of FPGA. Either, SynDEx's heuristic needs additional developments to optimize time reconfiguration. Furthermore, complex design and architecture can support more than one dynamic part.

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